step 86 and Fig. 5I, a fifth dielectric layer 154, for example FOX, is created in areas of the substrate where the third dielectric layer 146 is not located. Then in step 88, the patterned third dielectric layer 146 is removed, for example with an oxide strip.

In the Claims:

10. (Amended) A method of creating a substrate having multiple regions for creating low-voltage transistors of a first and second conductivity and high-voltage transistors of a first conductivity, [comprising]consisting essentially of the steps of:

creating a defined deposition of a first dielectric layer to expose a first region and a second region; [then consisting essentially of the steps of:]

implanting a first conductivity dopant into the first and second regions;

applying a first protective coating over the first and second regions;

driving in the first conductivity dopant into the substrate;

removing the first dielectric layer;

creating a defined deposition of a second dielectric layer in the same location as the defined deposition of the first dielectric layer;

implanting a second conductivity dopant in the substrate disposed under the defined deposition of the second dielectric layer;

driving in the second conductivity dopant into the substrate;

removing the first protective coating and the second dielectric layer;

creating a patterned third dielectric layer over the surface of the substrate to expose the drain and source of the first and second conductivity low-voltage transistors and the first conductivity high-voltage transistor;

creating a defined deposition of a fourth dielectric layer disposed on the drain and source of the first conductivity low-voltage transistor;

applying a second protective coating over the first and second regions;

implanting a second conductivity dopant into the substrate disposed under the drain and source of the first conductivity low-voltage transistor;

removing the second protective coating;

creating a fifth dielectric layer in areas of the substrate where the third dielectric layer is not located;

removing the patterned third dielectric layer; and

then further comprising the steps of:

creating a sixth dielectric layer over the surface of the substrate to form a gate oxide;

depositing a gate material over the sixth dielectric layer; and

patterning the sixth dielectric layer and the gate material to define gate regions of the first and second low conductivity transistors and a gate region of the first conductivity high-voltage transistor.

12. (Amended) A method of creating an integrated circuit having a second conductivity type low-voltage transistor in a first region, a first conductivity high-voltage transistor in a second region, and a first conductivity low-voltage transistor in a third region, comprising the steps of:

doping the first and second regions with a first dopant concentration to control the threshold voltage of the second conductivity low-voltage transistor; and

doping the third region with a second dopant concentration to control the threshold voltage of the first conductivity low-voltage transistor;

wherein an additional voltage threshold adjust implant step to adjust the threshold voltages of the first and second low-voltage transistors is not performed.

14. (Amended) A method of processing an integrated circuit having a second conductivity low-voltage transistor in a first region, a first conductivity high-voltage transistor in a third region, and a first conductivity low-voltage transistor in a second region, comprising the steps of:

doping the first and second regions with a first dopant concentration; and

doping the third region with a second dopant concentration; and

excluding the step of:

implanting an additional threshold voltage adjustment of the first and second low-voltage transistors; and

wherein the first and second regions have the substantially the same dopant concentration after processing of the integrated circuit.